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SUPPLEMENTAL APPEAL BRIEF FEE TRANSMITTAL		Attorney Docket No.	1614.1109
		Application Number	09/750,051
		Filing Date	December 29, 2000
		First Named Inventor	Shogo FUJIMORI et al.
		Group Art Unit	2123
AMOUNT ENCLOSED	500.00	Examiner Name	Dwin M. Craig

FEE CALCULATION (fees effective 12/08/04)

CLAIMS AS AMENDED	Claims Remaining After Amendment	Highest Number Previously Paid For	Number Extra	Rate	Calculations
TOTAL CLAIMS	22	- 22 =	0	X $ 50.00 =	$ 0.00
INDEPENDENT CLAIMS	3	- 3 =	0	X $ 200.00 =	0.00

Since an Official Action set an original due date of November 10, 2005, petition is hereby made for an extension to cover the date this reply is filed for which the requisite fee is enclosed (1 month ($120)); (2 months ($450)); (3 months ($1,020)); (4 months ($1,590)); (5 months ($2,160)):	
If Appeal Brief is enclosed, add ($500.00)	
If Statutory Disclaimer under Rule 20(d) is enclosed, add fee ($130.00)	
Information Disclosure Statement (Rule 1.17(p)) ($180.00)	
Total of above Calculations =	$
Reduction by 50% for filing by small entity (37 CFR 1.9, 1.27 & 1.28)	
TOTAL FEES DUE =	$

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(2) If entry (2) is less than 20, change entry (2) to "20".
(4) If entry (4) is less than entry (5), entry (6) is "0".
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SUBMITTED BY: STAAS & HALSEY LLP

Typed Name	Paul W. Bobowiec	Reg. No.	47,431
Signature	[signature]	Date	November 10, 2005

Docket No. 1614.1109

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Shogo FUJIMORI et al.

Application No.: 09/750,051 Group Art Unit: 2123

Confirmation No. 7012

Filed: December 29, 2000 Examiner: Dwin M. Craig

For: NOISE COUNTERMEASURE DETERMINATION METHOD AND APPARATUS AND STORAGE MEDIUM

APPEAL REINSTATEMENT REQUEST AND SUPPLEMENTAL APPEAL BRIEF UNDER 37 C.F.R §1.193(B)(2)

Mail Stop Appeal Brief-Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the Appellant's Notice of Appeal filed March 28, 2005, and the Examiner's reopening of prosecution in the Office Action mailed August 10, 2005, Appellant hereby requests reinstatement of the Appeal to the Board of Patent Appeals and Interferences.

In conformance with requirements set forth in 37 CFR §1.192(c), the Appeal Brief filed May 27, 2005 is incorporated herein by reference.

I. STATUS OF CLAIMS (37 CFR § 41.37(c)(1)(iii))

Pursuant to 37 C.F.R. §1.192(c)(3), claims 1-22 are pending in this application at the filing of this Appeal Brief.

Claims 1, 10, and 19 stand presently rejected under 35 U.S.C. §102(b) as being anticipated by Chian et al. (U.S.P. 5,682,336), claims 2, 3, 11, 12, 20-22 stand presently rejected under 35 U.S.C. §103(a) as being unpatentable over Chian in view of Tsuchida et al. (U.S.P. 5,559,997), and claims 7-8, 16 and 17 stand presently rejected over Chian in view of Petschauer et al. (U.S.P. 5,555,506).

Claims 4-6, 9, 13-15, and 18 stand presently objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Prior to the recently issued Office Action of August 10, 2005, claims 1-3, 7-12, and 16-22 stood rejected under 35 U.S.C. §102(b) as anticipated by Tsuchida (U.S.P. 5,559,997), claims 4 and 13 stood rejected under 35 U.S.C. §103(a) as being unpatentable over Tsuchida in view of Dorf (The Electrical Engineering Handbook, Second Edition, Richard C. Dorf, Editor CRC Press, 1997), and claims 5-6 and 14-15 stood rejected under 35 U.S.C. §103(a) as being unpatentable over Tsuchida in view of Guo (U.S.P. 6,597,808).

The outstanding Supplemental Appeal Brief addresses the new rejections presented by the Examiner in the Office Action mailed August 10, 2005.

II. STATUS OF AMENDMENTS (37 CFR § 41.37(c)(1)(iv))

No amendments have been filed subsequent to the final rejection made on March 14, 2005.

III. SUMMARY OF INVENTION (37 CFR § 41.37(c)(1)(v))

Claim 1 recites a noise countermeasure determination method (FIG. 3, pages 14-15). The method of claim 1 includes calculating recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis (step 3 illustrated in FIG. 3, pages 14-15). Claim 1 also recites a method comparing the input circuit information

and the recommended circuit information (step 5 illustrated in FIG. 3, pages 14-15). Claim 1 also recites a method determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures (step 5 illustrated in FIG. 3, pages 14-15).

Claim 10 recites a noise countermeasure determination apparatus (FIG. 1, pages 12-13). The apparatus of claim 10 includes a recommended circuit information calculating section calculating recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis (step 3 illustrated in FIG. 4 and pages 15-17). The apparatus of claim 10 also includes a noise countermeasure determination section comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures (step 5 illustrated in FIG. 4 and pages 15-17).

Claim 19 recites a computer-readable storage storing a program for controlling a computer to determine noise countermeasures by calculating recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis. (FIG. 1, pages 12, 13). Claim 19 also recites a computer-readable storage storing a program for controlling a computer to determine noise countermeasures by comparing the input circuit information and the recommended circuit information and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures (step 5 illustrated in FIG. 4 and pages 15-17).

IV. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 CFR § 41.37(c)(1)(vi))

Claims 1, 10, and 19 stand presently rejected under 35 U.S.C. §102(b) as being anticipated by Chian, claims 2, 3, 11, 12, and 20-22 stand presently rejected under 35 U.S.C. §103(a) as being unpatentable over Chian in view of Tsuchida, and claims 7-8, 16 and 17 stand presently rejected over Chian in view of Petschauer.

V. ARGUMENT OF EACH GROUND OF REJECTION PRESENTED FOR REVIEW (37 CFR § 41.37(c)(1)(vii))

All arguments are directed to the grounds of rejection. All citations to "current Office Action" refer to the Office Action mailed August 10, 2005.

A. Claim 1

In page 4, item 4.1, the Examiner cites Chian as providing these features. More specifically, the Examiner cites FIGs. 2 and 5 and col. 4, line 55 and col. 5, lines 25 and 38. As discussed below, Chain does not teach the features of claim 1 for which it is cited.

1. Features Not Discussed By Cited Art

To establish anticipation under §102, the prior art must teach each and every feature recited in the claim. See Manual Of Patent Examining Procedure § 2131 (8th ed. Rev. 2 May 2004)("MPEP"); *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

<u>Determining Noise Countermeasures Not Discussed in Chian</u>

Claim 1 recites a noise countermeasure determination method "<u>comparing</u> the input circuit information and the recommended circuit information, and <u>determining</u> a differing portion of the recommended circuit information differing from the input circuit information, as <u>noise countermeasures</u>." (Emphasis added).

Instead, Chian merely teaches (col. 5, lines 39-44):

> (i)n particular, in query step 53, if the noise performance output of the analysis of step 52 satisfies a prescribed noise performance criterion, the process proceeds to step 54, wherein the circuit is fabricated.

That is, Chian does not teach how the "noise reduction components" (that is, noise countermeasures) are determined. Rather, Chian merely teaches a judging in step 53 whether noise is within a tolerable range. That is, Chian merely judges whether an analyzed noise performance of an electronic circuit model satisfies a prescribed noise performance criterion.

The Examiner also refers to FIG. 2 of Chian as teaching "calculating recommended circuit information considered to minimize a noise by use of at least one formula."

However, FIG. 2 of Chian is merely used to illustrate (col. 2, lines 50-51) a circuit including a noise source. Thus, Chian does not illustrate the "circuit information considered to minimize a noise."

Thus, the rejection is incorrect since the cited art does not teach features recited by claim 1.

B. Claims 10 and 19

Claims 10 and 19 are patentable over the cited art, for reasons similar to those discussed above for claim 1. Claims 10 and 19 are similar to claim 1, but respectively specify a noise countermeasure determination apparatus and a computer-readable storage storing a program for controlling a computer to determine noise countermeasures including, using claim 10 as an example, "a noise countermeasure determination section comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures."

As discussed above with reference to claim 1, the rejection is incorrect since none of the cited art discusses each feature recited in claim 1 including comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures.

C: Claims 2-3, 11-12, and 20-22

As discussed above with reference to claim 1, Chian does not discuss comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures.

Claims 2-3, 11-12, and 20-22 more specifically recite respectively a noise countermeasure determination method and apparatus, or features thereof. Claim 2 recites a noise countermeasure determination method "further comprising: creating a simulation model of the input circuit information after determining the noise countermeasures; carrying out a circuit simulation using the simulation model, to calculate a signal waveform propagating through a wiring of the target circuit and to check whether or not a noise exceeding a tolerable range exists in the signal waveform; and categorizing the noise existing as a result of the noise check, and optimizing the determined noise countermeasures to only portions related to the noise."

Claim 3 recites a noise countermeasure determination "wherein the calculating recommended circuit information comprises outputting a range of a damping resistance as the recommended circuit information, based on a minimum voltage VIH-1 and a maximum voltage

VIH-2 which guarantee a normal operation of the target circuit, by taking a damping resistance which makes a first rising voltage of an input waveform at a receiving end of the target circuit equal to the minimum voltage VIH-1 as a maximum value of the range, and taking a damping resistance which makes the first rising voltage of the input waveform at the receiving end of the target circuit equal to the maximum voltage VIH-2 as a minimum value of the range."

Claim 11 recites a noise countermeasure determination apparatus "further comprising: a circuit model creating section creating a simulation model of the input circuit information after determining the noise countermeasures in said noise countermeasure determination section; a simulation and check section carrying out a circuit simulation using the simulation model, to calculate a signal waveform propagating through a wiring of the target circuit and to check whether or not a noise exceeding a tolerable range exists in the signal waveform; and a noise countermeasure optimizing section categorizing the noise existing as a result of the noise check carried out in said simulation and check section, and optimizing the determined noise countermeasures to only portions related to the noise."

Claim 12 further recites a noise countermeasure determination apparatus "wherein said recommended circuit information calculating section outputs a range of a damping resistance as the recommended circuit information, based on a minimum voltage VIH-1 and a maximum voltage VIH-2 which guarantee a normal operation of the target circuit, by taking a damping resistance which makes a first rising voltage of an input waveform at a receiving end of the target circuit equal to the minimum voltage VIH-1 as a maximum value of the range, and taking a damping resistance which makes the first rising voltage of the input waveform at the receiving end of the target circuit equal to the maximum voltage VIH-2 as a minimum value of the range."

Claim 20 recites a noise countermeasure determination method "further comprising carrying out at least one of a circuit rule check and a wiring topology check with respect to the input circuit information."

Claim 21 recites a noise countermeasure determination method "further comprising outputting an advice based on a check result obtained." Claim 22 recites a noise countermeasure determination method "further comprising correcting the input circuit information based on the advice output."

In page 3 of the current Office Action entitled "Response to Arguments", the Examiner contends that "it is inherent that the Tsuchida reference teaches characterizing a noise reduction

component, otherwise the component could not be added to the circuit layout simulation."

Appellant submits that this Examiner's Assertion is made in response to the Appellant's argument that "Tsuchida merely relates to a method of designing a printed-circuit (PC) board based on fundamental circuit design and the "noise reduction components" (that is, noise countermeasures)that are input" on page 4, lines 22-24 of the Appeal Brief.

However, as argued on page 3, lines 28-30 of the Appeal Brief, "Tsuchida merely determines whether to insert a noise reduction component within a limited range based on a predetermined rule, and does not teach how the "noise reduction components "(that is, noise countermeasures) may be determined.

In other words, Tsuchida merely describes inputting the "noise reduction components" (that is, noise countermeasures), and does not teach how such "noise reduction components" (that is, noise countermeasures) may be determined.

Accordingly, although the Examiner acknowledges that Tsuchida does not expressly disclose the use of at least one formula to model the noise signals being used to subject the at least one net of a target circuit to noise analysis and withdraws the rejection of the claims under 35 U.S.C. §102(b) as being anticipated by Tsuchida for this reason, it should be noted that Tsuchida <u>also</u> does not teach how the "noise reduction components" (that is, noise countermeasures), used by the method of designing the printed-circuit (SC) board, together with the fundamental circuit design, may be determined.

Further, with regard to claim 2 and 11, even an *arguendo* combination of claim 2 and 11 do not teach "categorizing the noise existing as a result of the noise check, and optimizing the determined noise countermeasures to only portions related to the noise."

Further, the basis for combining the prior art references of Chien and Tsuchida is the assumption that Tsuchida inherently "teaches characterizing a noise reduction component." As such the combination is improper.

As discussed above with reference to claims 1 and 10, the rejection is incorrect since none of the cited art teach features recited by claims 2-3, 11-12, and 20-22 further defining the method and apparatus recited by claims 1 and 10.

D. Claims 7-8, 16, and 17

As discussed above with reference to claims 1 and 10, Chian does not teach comparing

the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures.

Claims 7-8 and 16-17 more specifically recite a noise countermeasure determination apparatus, or the features thereof.

Claim 7 recites a noise countermeasure determination method "further comprising: creating a simulation model of input circuit information made up of circuit information of a target net which is to be subjected to the noise analysis and circuit information of an adjacent net which is adjacent to the target net, after determining the noise countermeasures carrying out a circuit simulation using the simulation model, to obtain a noise combined waveform by combining a crosstalk noise waveform and a signal waveform propagating through the target net which are calculated, and to check whether or not a noise exceeding a tolerable range exists based on the noise combined waveform; and categorizing the noise existing as a result of the noise check and optimizing the determined noise countermeasures to only portions related to the noise."

Claim 8 recites a noise countermeasure determination method "wherein said creating a simulation model creates the simulation model by assuming that the circuit information of the adjacent net is related to a net which has the same structure as the target net and is adjacent to the target net with a constant pattern gap formed therebetween."

Claim 16 recites a noise countermeasure determination apparatus "further comprising: a circuit model creating section creating a simulation model of input circuit information made up of circuit information of a target net which is to be subjected to the noise analysis and circuit information of an adjacent net which is adjacent to the target net, after determining the noise countermeasures by said noise countermeasure determination section; a simulation and check section carrying out a circuit simulation using the simulation model, to obtain a noise combined waveform by combining a crosstalk noise waveform and a signal waveform propagating through the target net which are calculated, and to check whether or not a noise exceeding a tolerable range exists based on the noise combined waveform; and a noise countermeasure optimizing section categorizing the noise existing as a result of the noise check carried out by said simulation and check section, and optimizing the determined noise countermeasures to only portions related to the noise.

Claim 17 recites a "noise countermeasure determination apparatus as claimed in claim

16, wherein said circuit model creating section creates the simulation model by assuming that the circuit information of the adjacent net is related to a net which has the same structure as the target net and is adjacent to the target net with a constant pattern gap formed therebetween."

Claim 18 recites a noise countermeasure determination apparatus "wherein processes of said circuit model creating section and said simulation and check section are repeated while changing the pattern gap, so as to obtain a minimum pattern gap with which the noise obtained as a result of the noise check carried out by said simulation and check section does not exceed the tolerable range, and said noise countermeasure determination section determines the minimum pattern gap as the noise countermeasures."

As discussed above with reference to claims 1 and 10, the rejection is incorrect since none of the cited art teach features recited by claims 7-8 and 16-17 further defining the method recited by claim 1 and the apparatus recited by claim 10.

E. Claims 4-6, 9, 13-15, and 18 are indicated as being allowable if rewritten in independent form.

Since the independent claims 1 and 10 from which these claims 4-6, 9, 13-15 and 18 depend upon are clearly patentable over the prior art as discussed above, it is believed that these claims 4-6, 9, 13-15 and 18 are allowable in their dependent form.

VI. CONCLUSION

In summary, Appellant submits that all pending claims 1-22 patentably distinguish over the prior art. Reversal of the Examiner's rejection is respectfully requested.

In view of the law and facts stated herein, the Appellant respectfully submits that the Examiner has failed set to forth anticipatory and obviousness cases against the pending claims.

For all the foregoing reasons, the Appellant respectfully submits that the cited prior art does not teach the presently claimed invention.

The claims are patentable over the prior art of record and the Examiner's findings of unpatentability regarding claims 1-22 should be reversed and the patentability over the presently cited references be affirmed.

The Commissioner is hereby authorized to charge any additional fees required in connection with the filing of the previous Appeal Brief and the outstanding Supplemental Appeal

Brief to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: November 10, 2005

By Paul W. Bobowiec
Paul W. Bobowiec
Registration No. 47,431

1201 New York Ave, N.W., Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501

CLAIMS APPENDIX (37 CFR § 41.37(c)(1)(viii))

1. (PREVIOUSLY PRESENTED) A noise countermeasure determination method comprising:

calculating recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis; and

comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures.

2. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 1, further comprising:

creating a simulation model of the input circuit information after determining the noise countermeasures;

carrying out a circuit simulation using the simulation model, to calculate a signal waveform propagating through a wiring of the target circuit and to check whether or not a noise exceeding a tolerable range exists in the signal waveform; and

categorizing the noise existing as a result of the noise check, and optimizing the determined noise countermeasures to only portions related to the noise.

3. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 1, wherein the calculating recommended circuit information comprises outputting a range of a damping resistance as the recommended circuit information, based on a minimum voltage VIH-1 and a maximum voltage VIH-2 which guarantee a normal operation of the target circuit, by taking a damping resistance which makes a first rising voltage of an input waveform at a receiving end of the target circuit equal to the minimum voltage VIH-1 as a maximum value of the range, and taking a damping resistance which makes the first rising voltage of the input waveform at the receiving end of the target circuit equal to the maximum voltage VIH-2 as a minimum value of the range.

4. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 3, wherein the calculating recommended circuit information comprises:

comparing a damping resistance which makes a voltage at a time of a ringback equal to

the minimum voltage VIH-1 and the minimum value of the damping

resistance, and

outputting a larger one of the compared values as the minimum value of the damping resistance.

5. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 1, further comprising outputting input circuit information that includes a wiring length that is substantially a Manhattan distance that is determined based on positions of part pins forming the target circuit and a wiring topology.

6. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 5, further comprising:

creating a simulation model of the input circuit information after determining the noise countermeasures;

carrying out a circuit simulation using the simulation model, to calculate a signal waveform propagating through a wiring of the target circuit and to check whether or not a noise exceeding a tolerable range exists in the signal waveform; and

repeating the creating a simulation model and the carrying out a circuit simulation using the simulation model using a plurality of wiring topologies, and determining an optimum wiring topology from results of the noise check carried out in said carrying out a circuit simulation using the simulation model to use in said, outputting input circuit information so that the optimum wiring topology is determined as the noise countermeasures in said comparing the input circuit information and the recommended circuit information.

7. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 1, further comprising:

creating a simulation model of input circuit information made up of circuit information of a target net which is to be subjected to the noise analysis and circuit information of an adjacent net which is adjacent to the target net, after determining the noise countermeasures

carrying out a circuit simulation using the simulation model, to obtain a noise combined waveform by combining a crosstalk noise waveform and a signal waveform propagating through the target net which are calculated, and to check whether or not a noise exceeding a tolerable range exists based on the noise combined waveform; and

categorizing the noise existing as a result of the noise check

and optimizing the determined noise countermeasures to only portions related to the noise.

8. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 7, wherein said creating a simulation model creates the simulation model by assuming that the circuit information of the adjacent net is related to a net which has the same structure as the target net and is adjacent to the target net with a constant pattern gap formed therebetween.

9. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 8, wherein said creating a simulation model and said carrying out a circuit simulation using the simulation model are repeated while changing the pattern gap, so as to obtain a minimum pattern gap with which the noise obtained as a result of the noise check carried out in said carrying out a circuit simulation using the simulation model

does not exceed the tolerable range, and said comparing the input circuit information and the recommended circuit information determines the minimum pattern gap as the noise countermeasures.

10. (ORIGINAL) A noise countermeasure determination apparatus comprising:

a recommended circuit information calculating section calculating recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis; and

a noise countermeasure determination section comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures.

11. (ORIGINAL) The noise countermeasure determination apparatus as claimed in claim 10, further comprising:

a circuit model creating section creating a simulation model of the input circuit information after determining the noise countermeasures in said noise countermeasure determination section;

a simulation and check section carrying out a circuit simulation using the simulation

model, to calculate a signal waveform propagating through a wiring of the target circuit and to check whether or not a noise exceeding a tolerable range exists in the signal waveform; and a noise countermeasure optimizing section categorizing the noise existing as a result of the noise check carried out in said simulation and check section, and optimizing the determined noise countermeasures to only portions related to the noise.

12. (ORIGINAL) The noise countermeasure determination apparatus as claimed in claim 10, wherein said recommended circuit information calculating section outputs a range of a damping resistance as the recommended circuit information, based on a minimum voltage VIH-1 and a maximum voltage VIH-2 which guarantee a normal operation of the target circuit, by taking a damping resistance which makes a first rising voltage of an input waveform at a receiving end of the target circuit equal to the minimum voltage VIH-1 as a maximum value of the range, and taking a damping resistance which makes the first rising voltage of the input waveform at the receiving end of the target circuit equal to the maximum voltage VIH-2 as a minimum value of the range.

13. (ORIGINAL) The noise countermeasure determination apparatus as claimed in claim 12, wherein said recommended circuit information calculating section compares a damping resistance which makes a voltage at a time of a ringback equal to the minimum voltage VIH-1 and the minimum value of the damping resistance, and outputs a larger one of the compared values as the minimum value of the damping resistance.

14. (PREVIOUSLY PRESENTED) The noise countermeasure determination apparatus as claimed in claim 10, further comprising:

a circuit information output section outputting input circuit information that includes a wiring length that is substantially a Manhattan distance that is determined based on positions of part pins forming the target circuit and a wiring topology.

15. (PREVIOUSLY PRESENTED) The noise countermeasure determination apparatus as claimed in claim 13, further comprising:

a circuit model creating section creating a simulation model of the input circuit information after determining the noise countermeasures in said noise countermeasure determination section; and

a simulation and check section carrying out a circuit simulation using the simulation

model, to calculate a signal waveform propagating through a wiring of the target circuit and to check whether or not a noise exceeding a tolerable range exists in the signal waveform

wherein processes of said circuit model creating section and said simulation and check section being repeated using a plurality of wiring topologies, and an optimum wiring topology being determined from results of the noise check carried out by said simulation and check section for use by said circuit model creating section, so that the optimum wiring topology is determined as the noise countermeasures by said noise countermeasure determination section.

16. (ORIGINAL) The noise countermeasure determination apparatus as claimed in claim 10, further comprising:

a circuit model creating section creating a simulation model of input circuit information made up of circuit information of a target net which is to be subjected to the noise analysis and circuit information of an adjacent net which is adjacent to the target net, after determining the noise countermeasures by said noise countermeasure determination section;

a simulation and check section carrying out a circuit simulation using the simulation model, to obtain a noise combined waveform by combining a crosstalk noise waveform and a signal waveform propagating through the target net which are calculated, and to check whether or not a noise exceeding a tolerable range exists based on the noise combined waveform; and

a noise countermeasure optimizing section categorizing the noise existing as a result of the noise check carried out by said simulation and check section, and optimizing the determined noise countermeasures to only portions related to the noise.

17. (ORIGINAL) The noise countermeasure determination apparatus as claimed in claim 16, wherein said circuit model creating section creates the simulation model by assuming that the circuit information of the adjacent net is related to a net which has the same structure as the target net and is adjacent to the target net with a constant pattern gap formed therebetween.

18. (ORIGINAL) The noise countermeasure determination apparatus as claimed in claim 17,

wherein processes of said circuit model creating section and said simulation and check section are repeated while changing the pattern gap, so as to obtain a minimum pattern gap with which the noise obtained as a result of the noise check carried out by said simulation and check section does not exceed the tolerable range, and said noise countermeasure determination section determines the minimum pattern gap as the noise countermeasures.

19. (PREVIOUSLY PRESENTED) A computer-readable storage storing a program for controlling a computer to determine noise countermeasures, by:

calculating recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis; and

comparing the input circuit information and the recommended circuit information and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures.

20. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 1, further comprising carrying out at least one of a circuit rule check and a wiring topology check with respect to the input circuit information.

21. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 20, further comprising outputting an advice based on a check result obtained.

22. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 21, further comprising correcting the input circuit information based on the advice output.